A 10-Bit High-Speed SAR A/D Converter

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Abstract: *An Hybrid technique to the circuit implementation of 10-bit analog-to-digital converter(ADC) is proposed. This method demonstrates a simple technique to increase speed of successive approximation ADC's that require as few as 2 comparisons for 10 bit conversion. This technique needs only $1/4^{th}$ conversion time of conventional successive approximation ADC. The approach divides input range into 256-quantization cells, separated by 255 boundary points; an 8-bit binary code 00000000 to 11111111 is assigned to each cell. A normal successive approximation converter requires 10 comparisons for 10-bit quantization, while our proposed technique reduces number of comparison requirements to 2 comparisons. An experimental prototype of 10-bit ADC using proposed technique was implemented using µp 8085. Use of Microprocessor has greatly reduced the hardware requirement and cost. This technique is best suitable when high speed combined with high resolution is required. The ADC Results of 10-bit prototype is presented. The results show that the ADC exhibits a maximum DNL of 0.47LSB and a maximum INL of 0.5LSB.*

Keywords: *Analog to digital converter, digital to analog converter, flash ADC, Microprocessor, Successive approximation.*

I. Introduction

Analog-to-digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses 2^N -1 comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions [2]. All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially and consequently this architecture requires very large IC's. It has high power dissipation. The conventional pipelined architecture has been widely employed to meet the required performance in this arena due to properly managed trade-offs between speed, power consumption and die area [3-5]. Among a variety of pipelined ADCs, the multi bit-per-stage architecture is more suitable for high resolution, as the single bit- per stage structure requires more stages, high power consumption and larger chip area [6]. However the multi bit-per-stage architecture has a relatively low signal processing speed due to reduced feedback factor in the closed – loop configuration of the amplifiers. In switched capacitor type multiplying digital-to-analog converters (MDACS) used in conventional pipelined ADCs, the mismatch between capacitors limits the differential nonlinearly (DNL) of ADCs. This is because each DNL step is defined by the random process variation of each unit capacitor value. A common centroid geometry layout technique can improve this capacitor matching for DNL, but it cannot have an effect on random mismatch [7]. Naturally, increasing the capacitor size can directly improve the capacitor matching accuracy, but at the added cost of increased load capacitance. This means the amplifiers would dissipate more power or the ADC sampling speed would have to be reduced. Two step Flash converters are popular for conversion resolutions in the 8-10 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [8, 9]. However, beyond such resolution, the area and power dissipation of two-step flash ADC's nearly double for each additional bit of resolution [10]. There are many different architectures like pipelined convertor [11, 12], successive approximation convertor [13, 14], Sigma-Delta convertor [15], folding ADC's [16], reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper a simple hybrid technique for the circuit implementation of 10-bit analog-to-digital (A/D) converter is proposed, This method demonstrates a simple technique to increase speed of successive approximation ADC's that require as few as 2 comparisons for 10 bit conversion.

II. Flash ADC

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters consume considerable power, have relatively low resolution, and can be quite

expensive. This limits them to high frequency applications that typically cannot be addressed any other way. Typical examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.
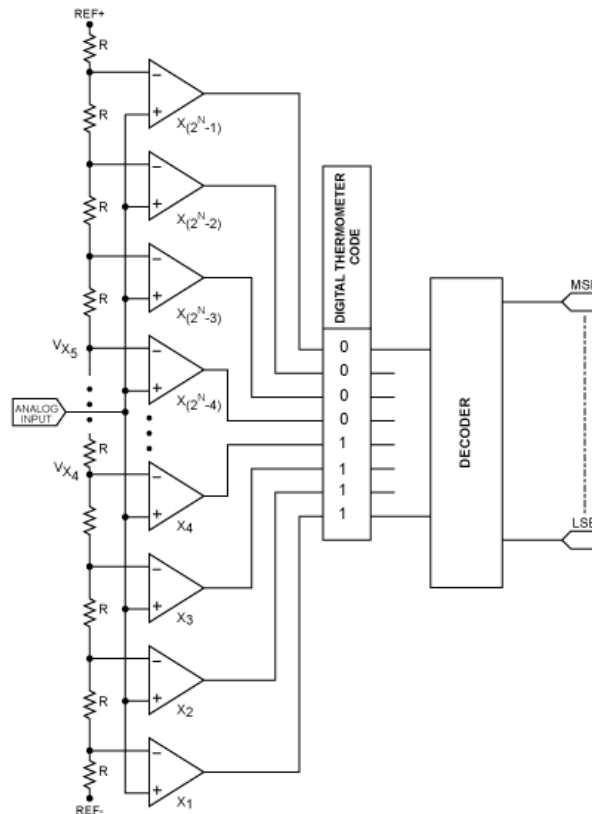

Figure 1: Flash ADC architecture.

2.1 Architectural Details

Flash ADCs are made by cascading high-speed comparators. Fig. 1 shows a typical flash ADC block diagram. For an N-bit converter, the circuit employs $2^N - 1$ comparators. A resistive-divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0. Thus, if the analog input is between V_{X4} and V_{X5}, comparators X_1 through X_4 produce 1s and the remaining comparators produce 0s. The point where the code changes from ones to zeros is the point at which the input signal becomes smaller than the respective comparator reference-voltage levels. If the analog input is between V_{X4} and V_{X5}, comparators X_1 through X_4 produce 1s and the remaining comparators produce 0s. This architecture is known as thermometer code encoding. This name is used because the design is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code.

The comparators are typically a cascade of wideband low gain stages. They are low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. The comparators are designed for low-voltage offset, so that the input offset of each comparator is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code that is not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a 1 or a 0.

III. SAR ADC

Successive approximation ADCs are widely used for high resolution, medium speed 5MS/s, low-power, low-cost applications such as automotive, factory automation, and pen digitizer applications [17-21]. Successive approximation ADCs with improved performance, lower cost, and higher reliability can make a significant impact in industry.

3.1 Configuration Of Successive Approximation ADC

A conventional successive approximation ADC consists of a track-hold circuit, a comparator, a DAC, successive approximation logic and time-base circuits Fig. 2 shows a typical block diagram of successive approximation ADC. The track-hold circuit, and ensuring linearity of DAC input output characteristics, is the most critical parts of the design. Usually a ring counter is used in the time-base circuitry to provide accurate timing signals.
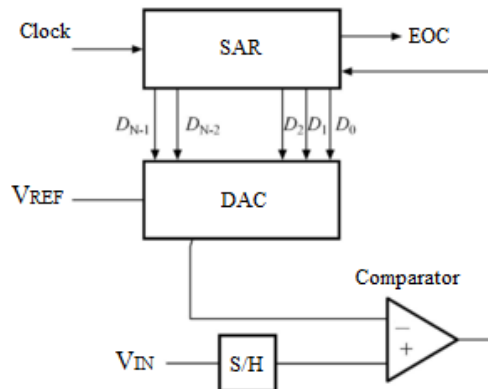

Figure 2: Block diagram of Successive approximation ADC

3.2 Operation Of Successive Approximation ADC

The successive approximation ADC operates according to a binary search algorithm as follows: The track-hold circuit samples and holds the voltage of the analog input Vin (full-scale input is Vref).The comparator compares the voltages of Vin (held by the track-hold circuit) and Vref /2 (where Vref /2 is generated by the DAC).In case Vin >Vref/2: The comparator outputs logic "1".The comparator then compares the voltage Vin with (3/4)Vref (where (3/4)Vref is generated by the DAC).If Vin > (3/4)Vref, then (7/8)Vref is used for the next comparison. Else if Vin < (3/4)Vref, then (5/8)Vref is used. This binary search continues in this manner. In case Vin<Vref /2: The comparator outputs logic"0".The comparator then compares the voltages Vin with (1/4)Vref (where (1/4)Vref is generated by the DAC).If Vin > (1/4)Vref, then (3/8)Vref is used for the next comparison. Else if Vin < (1/4)Vref, then (1/8)Vref is used. The successive approximation ADC performs N comparisons, then outputs a digital value corresponding to the N-bit binary comparison result.

IV. Proposed ADC Architecture

Flash ADC's are promising for high Speed applications. However, these ADC's are unsuitable for high resolution applications. The number of comparators grows exponentially with resolution, and consequently this architecture requires very large IC's and it has high power dissipation. The ADC based on our technique enjoys the benefit of employing only 256 comparators, instead of 1024 comparators normally required in conventional 10-bit flash architecture, while maintaining the advantage of high speed. The block diagram of 10-bit ADC using proposed technique is illustrated in Fig. 3. The ADC consists of an input sample and hold amplifier (SHA), 8-bit flash ADC, 10-bit DAC, 8-bit µp 8085, 8:16 bit MUX/DEMUX switch and some extra supporting circuit blocks. 8-bit flash ADC, partitions input range into 256-quantization cells, separated by 255 boundary points. An 8-bit binary code 00000000 to 11111111 is assigned to each cell. The µp 8085 decides within which cell the input sample lies and assigns a 10-bit binary center code according to the cell value. The exact 10-bit digital code for analog sample is obtained by successive approximation technique.

4.1 Circuit Implementation

The block diagram of the 10-bit ADC is as shown in Fig. 3. The Microprocessor port A is used as input port, which gets the 8-bit code from 8-bit flash ADC, corresponding center value 10-bit binary code of a particular cell is loaded into the accumulator. Port C is used as output port, connected to 10-bit DAC through 8:16 bit switch to obtain analog signal equivalent to digital count in register A, which is compared with an analog input voltage V_{IN}. Equivalent 10-bit digital code for analog input signal is obtained by successive approximation technique. The conversion algorithm is similar to the binary search algorithm. First, the reference voltage of a particular cell, Vref (DAC) provided by DAC is set to V_N / 2 to obtain the MSB, where V_N is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with V_N/4 or 3/4*V_N depending on the result of the MSB. If the MSB is "1", then Vref (DAC) = ¾*V_N, otherwise Vref (DAC) =V_N/4. This sequence will continue until the LSB is obtained. To get a 10-bit digital output, 2 comparisons are needed. Finally 10-bit digital code is available at

8:16 bit switch software for implementing successive approximation converter in Microprocessor is written in assembler code and converted to hex code by assembler software. Hex codes are transferred to Microprocessor by programmer.
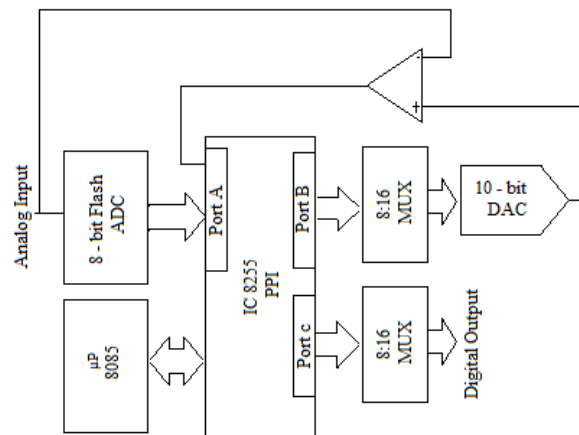

Figure 3: Block Diagram of 10-bit ADC

V. Measured Result

An experimental prototype of 10-bit ADC using proposed technique was designed and developed using μP8085. The working functionality of the ADC has been checked by applying a ramp input going from 0 to 3.5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 1024 for 10-bit at the output, indicating that the ADC's working is functionally correct. Both the differential and integral nonlinearities (DNL and INL) were measured over 2^{10} output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 1023 steps .The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.49LSB and a maximum INL of 0.51LSB as shown in the Figs. 4(a) and 4(b).
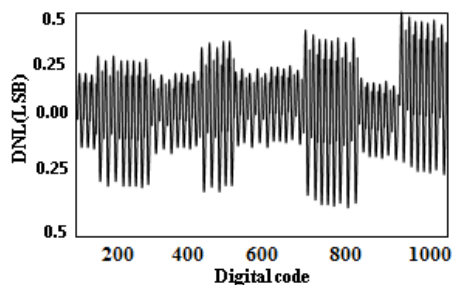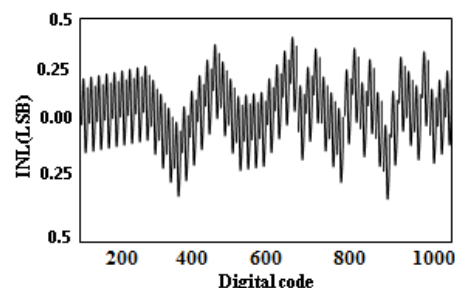

Figure 4(a): DNL Versus output Code

Figure 4(b): INL Versus output Code

VI. Conclusion

We have presented a simple and effective technique for enhancing speed of 10-bit SAR ADC. This technique Would be effective in a large number of high speed controls and signal processing applications such as hard disk- drive read Chanel and wireless receivers. Although, these applications are most often implemented with flash convertors but these ADC's demands larger power. And also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10-bits. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10-bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high speed applications, with less power dissipation even beyond 10-bit resolution. Implementation of successive approximation algorithm using Microprocessor has reduced the hardware requirement and cost. Proposed technique uses only 256 comparators for 10-bit resolution.

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